What is claimed is:

1. A method of fabricating an ultra shallow junction of a field effect transistor, comprising:

(a) supplying a substrate comprising a gate structure of the transistor;

(b) etching a surface of the substrate in source and drain regions of the transistor;

(c) selectively forming a protective film on said surface of the substrate;

(d) laterally etching the substrate beneath a gate dielectric of the gate structure; and

(e) removing the protective film.

2. The method of claim 1 wherein the substrate is a silicon wafer.

3. The method of claim 1 wherein the gate structure comprises the gate dielectric and a gate electrode formed on the gate dielectric.

4. The method of claim 1 wherein the step (b) further comprises:
providing Cl_2 and HBr at a flow ratio Cl_2:HBr in a range from about 1:15 to 15:1.

5. The method of claim 1 wherein the step (d) further comprises:
providing HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from about 1:15 to 15:1.

6. The method of claim 1 wherein the step (c) further comprises:
oxidizing portions of said regions of the transistor.

7. The method of claim 6 further comprising:
providing a directional oxygen plasma using a cathode bias of 20 to 200 W.

8. The method of claim 6 wherein the step (e) further comprises:
providing carbon tetrafluoride (CF_4) at a flow rate of 50 sccm, applying 500 W of power to the inductively coupled antenna, applying 40 W of bias power to the cathode and maintaining a wafer temperature of 50 degrees at a chamber pressure of 4 mtorr.

9. The method of claim 1 wherein the step (c) further comprises:
depositing a silicon dioxide layer on portions of said regions of the transistor.

10. The method of claim 9 wherein the step (e) further comprises:
providing carbon tetrafluoride (CF_4) at a flow rate of 50 sccm, applying 500 W of power to the inductively coupled antenna, applying 40 W of bias power to the cathode and maintaining a wafer temperature of 50 degrees at a chamber pressure of 4 mtorr.

11. The method of claim 1 wherein the step (c) further comprises:
depositing a carbon layer on portions of said regions of the transistor.

12. The method of claim 11 wherein the step (e) further comprises:
providing O_2 and Ar at a flow ratio O_2:Ar in a range from about 1:20 to 20:1.

13. The method of claim 1 wherein the step (e) further comprises removal of residue.

14. The method of claim 13 further comprising:
providing CF_4 and H_2O at a flow ratio CF_4:H_2O in a range from about 1:10 to 10:1.

15. The method of claim 1 further comprising:
depositing doped epitaxial films to form a source and a drain of the transistor.

16. A method of fabricating an ultra shallow junction of a field effect transistor, comprising:

supplying a silicon substrate comprising a gate structure of the transistor;

etching a surface of the substrate in source and drain regions of the transistor by providing Cl_2 and HBr at a flow ratio Cl_2:HBr of 10:1, applying 350 W to an inductively coupled antenna and 40 W of substrate bias power, and maintaining the substrate at 45 degrees Celsius at a chamber pressure of 25 mTorr;

forming a protective film on portions of said etched surface using a directional oxygen plasma, a cathode bias of 20 to 200 W and maintaining the substrate at 50

degrees Celsius at a chamber pressure of 10 mTorr;

laterally etching the substrate beneath a gate dielectric of the gate structure by providing HBr and Cl_2 at a flow ratio HBr:Cl_2 of about 3:1 and 30 % by volume of oxygen (O_2) in helium (He) at a rate of 6 sccm, applying 700 W to an inductively coupled antenna and 65 W of substrate bias power, and maintaining the substrate at 50 degrees Celsius at a chamber pressure of 70 mTorr;

removing the protective film by providing carbon tetrafluoride (CF_4) at a flow rate of 50 sccm, applying 500 W of power to the inductively coupled antenna, applying 40 W of bias power to the cathode and maintaining a wafer temperature of 50 degrees at a chamber pressure of 4 mtorr;

removing residue by dipping the substrate in an aqueous solution including hydrogen fluoride, and

depositing doped epitaxial films into the etched portions of the substrate to form a source and a drain of the transistor.

17. A method of fabricating an ultra shallow junction of a field effect transistor, comprising:

supplying a silicon substrate comprising a gate structure of the transistor;

etching a surface of the substrate in source and drain regions of the transistor by providing Cl_2 and HBr at a flow ratio Cl_2:HBr of 10:1, applying 350 W to an inductively coupled antenna and 40 W of substrate bias power, and maintaining the substrate at 45 degrees Celsius at a chamber pressure of 25 mTorr;

depositing a silicon oxide protective film on portions of said etched surface;

laterally etching the substrate beneath a gate dielectric of the gate structure by providing HBr and Cl_2 at a flow ratio HBr:Cl_2 of about 3:1 and 30 % by volume of oxygen (O_2) in helium (He) at a rate of 6 sccm, applying 700 W to an inductively coupled antenna and 65 W of substrate bias power, and maintaining the substrate at 50 degrees Celsius at a chamber pressure of 70 mTorr;

removing the silicon oxide protective film by providing carbon tetrafluoride (CF_4) at a flow rate of 50 sccm, applying 500 W of power to the inductively coupled antenna, applying 40 W of bias power to the cathode and maintaining a wafer temperature of 50 degrees at a chamber pressure of 4 mtorr;

removing residue by dipping the substrate in an aqueous solution including hydrogen fluoride, and

depositing doped epitaxial films into the etched portions of the substrate to form a source and a drain of the transistor.

18. A method of fabricating an ultra shallow junction of a field effect transistor, comprising:

supplying a silicon substrate comprising a gate structure of the transistor;

etching a surface of the substrate in source and drain regions of the transistor by providing Cl_2 and HBr at a flow ratio Cl_2:HBr of 10:1, applying 350 W to an inductively coupled antenna and 40 W of substrate bias power, and maintaining the substrate at 45 degrees Celsius at a chamber pressure of 25 mTorr;

depositing an amorphous carbon protective film on portions of said etched surface;

laterally etching the substrate beneath a gate dielectric of the gate structure by providing HBr and Cl_2 at a flow ratio HBr:Cl_2 of about 3:1 and 30 % by volume of oxygen (O_2) in helium (He) at a rate of 6 sccm, applying 700 W to an inductively coupled antenna and 65 W of substrate bias power, and maintaining the substrate at 50 degrees Celsius at a chamber pressure of 70 mTorr;

removing the amorphous carbon protective film providing O_2 and Ar at a flow ratio O_2:Ar of about 0.75:1, applying 1000 W to an inductively coupled antenna and 100 W of substrate bias power, and maintaining the substrate at 45 degrees Celsius at a chamber pressure of 4 mTorr;

removing residue by dipping the substrate in an aqueous solution including hydrogen fluoride; and

depositing doped epitaxial films into the etched portions of the substrate to form a source and a drain of the transistor.

19. A computer-readable medium including software that, when executed by a processor, performs a method that causes a semiconductor substrate processing platform to fabricate an ultra shallow junction of a field effect transistor, comprising:

(a) supplying a substrate comprising a gate structure of the transistor;

(b) etching a surface of the substrate in source and drain regions of the transistor;

(c) selectively forming a protective film on said surface of the substrate;

(d) laterally etching the substrate beneath a gate dielectric of the gate structure;

and

(e) removing the protective film.

20. The computer-readable medium of claim 19 wherein the step (b) further comprises:

providing Cl_2 and HBr at a flow ratio Cl_2:HBr in a range from about 1:15 to 15:1.

21. The computer-readable medium of claim 19 wherein the step (d) further comprises:

providing HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from about 1:15 to 15:1.

22. The computer-readable medium of claim 19 wherein the step (c) further comprises:

oxidizing portions of said regions of the transistor.

23. The computer-readable medium of claim 22 wherein the step (e) further comprises:

providing carbon tetrafluoride (CF_4) at a flow rate of 50 sccm, applying 500 W of power to the inductively coupled antenna, applying 40 W of bias power to the cathode and maintaining a wafer temperature of 50 degrees at a chamber pressure of 4 mtorr.

24. The computer-readable medium of claim 19 wherein the step (c) further comprises:

depositing a silicon oxide layer on portions of said regions of said transistor.

25. The computer-readable medium of claim 24 wherein the step (e) further comprises:

providing carbon tetrafluoride (CF_4) at a flow rate of 50 sccm, applying 500 W of power to the inductively coupled antenna, applying 40 W of bias power to the cathode and maintaining a wafer temperature of 50 degrees at a chamber pressure of 4 mtorr.

26. The computer-readable medium of claim 19 wherein the step (c) further comprises:

depositing an inorganic carbon layer on portions of said regions of the transistor.

27. The computer-readable medium of claim 26 wherein the step (e) further comprises:

providing O_2 and Ar at a flow ratio O_2:Ar in a range from about 1:20 to 20:1.

28. The computer-readable medium of claim 19 wherein the step (e) further comprises removal of residue.

29. The computer-readable medium of claim 28 further comprising:

dipping the substrate in an aqueous solution including hydrogen fluoride.

30. The computer-readable medium of claim 19 further comprising:

depositing doped epitaxial films to form a source and a drain of the transistor.